(1390 REV. 5-93) US DEPT. OF COMMERCE PATENT & TRADEMARK OFFICE		ATTORNEY'S DOCKET NUMBER 108572
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		U.S. APPLICATION NO. (if known, sec 37 C.F.R.1.5) 09/762589
INTERNATIONAL APPLICATION NO. PCT/GB00/02321	INTERNATIONAL FILING DATE June 15, 2000	PRIORITY DATE CLAIMED June 15, 1999

TITLE OF INVENTION
SEMICONDUCTOR DEVICE SIMULATION METHOD AND SIMULATOR

APPLICANT FOR DO/EO/US
Basil LUI

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.

2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.

3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).

4. ☐ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☒ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)

6. ☐ A translation of the International Application into English (35 U.S.C. 371(c)(2)).

7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.

8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).

9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).

10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.

12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.

13. ☒ A FIRST preliminary amendment.

    ☐ A SECOND or SUBSEQUENT preliminary amendment.

14. ☐ A substitute specification.

15. ☐ Entitlement to small entity status is hereby asserted.

16. ☐ Other items or information:

JC05 Rec'd PCT/PTO 09 FEB 200

U.S. APPLICATION NO. (if known, see 37 C.F.R. 1.5) 09/762589	INTERNATIONAL APPLICATION NO. PCT/GB00/02321	ATTORNEY'S DOCKET NUMBER 108572

17. ☒ The following fees are submitted:	CALCULATIONS	PTO USE ONLY
Basic National fee (37 CFR 1.492(a)(1)-(5)):		
Search Report has been prepared by the EPO or JPO $860.00		
International preliminary examination fee paid to USPTO (37 CFR1.482) $690.00		
No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) $710.00		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO.....$1,000.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) .....$ 100.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$860.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$	

Claims	Number Filed	Number Extra	Rate		
Total Claims	12 - 20 =	0	X $ 18.00	$	
Independent Claims	6 - 3 =	3	X $ 80.00	$240.00	
Multiple dependent claim(s)(if applicable)			+ $270.00	$	
TOTAL OF ABOVE CALCULATIONS =				$1100.00	
Reduction by 1/2 for filing by small entity, if applicable. -				$	
SUBTOTAL =				$1100.00	
Processing fee of $130.00 for furnishing the English translation later than ☐ 20 ☐ 30 month from the earliest claimed priority date (37 CFR 1.492(f)). +				$	
TOTAL NATIONAL FEE =				$1100.00	
				Amount to be refunded	$
				Charged	$

a. ☒ Check No. 116180 in the amount of $1100.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Director is hereby authorized to charge any additional fees which may be required, or credit any overpayment, to Deposit Account No. 15-0461. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

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(1390 Rev.10-00)

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Basil LUI

Application No.: New US National Stage of PCT/GB00/02321

Filed: February 9, 2001 Docket No.: 108572

For: SEMICONDUCTOR DEVICE SIMULATION METHOD AND SIMULATOR

PRELIMINARY AMENDMENT

Director of the U.S. Patent and Trademark Office
Washington, D. C. 20231

Sir:

Prior to initial examination, please amend the above-identified application as follows:

IN THE CLAIMS:

Please replace claims 4 and 8 as follows:

4. (Amended) A simulator as claimed in claim 1 which determines the leakage current in a polysilicon Thin Film Transistor.

8. (Amended) A simulator as claimed in claim 5 which determines the leakage current in a polysilicon Thin Film Transistor.

Please add new claims 9-12 as follows:

--9. A simulator as claimed in claim 2 which determines the leakage current in a polysilicon Thin Film Transistor.--

--10. A simulator as claimed in claim 3 which determines the leakage current in a polysilicon Thin Film Transistor.--

--11. A simulator as claimed in claim 6 which determines the leakage current in a polysilicon Thin Film Transistor.--

--12. A simulator as claimed in claim 7 which determines the leakage current in a polysilicon Thin Film Transistor.--

REMARKS

Claims 1-12 are pending. Claims 4 and 8 have been amended to eliminate multiple dependencies and claims 9-12 have been added to compensate for the subject matter deleted from claims 4 and 8. Prompt and favorable consideration on the merits is respectfully requested.

The attached Appendix includes marked-up copies of each rewritten claim (37 C.F.R. 1.121(c)(ii)).

Respectfully submitted,

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DEPOSIT ACCOUNT USE AUTHORIZATION
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APPENDIX

Changes to Claims:

The following are marked-up versions of the amended claims:

4. (Amended) A simulator as claimed in ~~any one of~~ claims 1 ~~to 3~~ which determines the leakage current in a polysilicon Thin Film Transistor.

8. (Amended) A simulator as claimed in ~~any one of~~ claims 5 ~~to 7~~ which determines the leakage current in a polysilicon Thin Film Transistor.

Semiconductor Device Simulation Method and Simulator

The present invention relates to an automated simulation method for determining the enhanced generation-recombination rate due to trap-to-band tunnelling in a semiconductor device using the Dirac coulombic tunnelling integral and to a simulator for carrying out the method.

The enhanced generation-recombination rate due to trap-to-band tunnelling in a semiconductor device is considered to be responsible for a number of important effects in semiconductor devices, including the anomalous leakage current in polysilicon Thin Film Transistors (TFTs). Polysilicon TFTs are widely used for example in active matrix display devices. The anomalous leakage current of the TFTs can severely degrade the pixel voltage in such display devices. Thus, this is one example of the commercial importance of an automated simulation method and simulator of the type provided by the present invention.

Having regard to the complexity and cost of the fabrication processes for manufacturing semiconductor devices, it is highly desirable if not essential for the design and performance evaluation of such devices to be undertaken using mathematical simulations, often referred to as modelling. It is clearly crucial for such modelling to be able to provide accurate calculation of the enhanced generation-recombination rate due to trap-to-band tunnelling, and hence the leakage current, within a semiconductor device. Consequently, considerable effort has previously been spent in developing methods of calculating the enhanced generation-recombination rate due to trap-to-band tunnelling in a semiconductor device. Such methods are embodied in computer programs which are sold as staple commercial products by or on behalf of their developers to designers and manufacturers of semiconductor devices.

In a paper submitted in 1996 and published in 1997 (Solid State Electronics Vol.41, No.4, pp 575-583 1997) the inventors hereof presented a generation-recombination model for device simulation including the Poole-Frenkel effect and phonon-assisted tunnelling. The model is conveniently referred to as the Dirac Coulombic Tunnelling Integral, which is recited as equation 1 in figure 9 hereof.

As noted in the above mentioned published paper, the Dirac Coulombic Tunnelling Integral is applicable to semiconductor devices generally. However, as also noted above, an important category of semiconductor devices is thin film transistors (TFTs) and such a device will herein after be used for ease of reference, but by way of one example only of a semiconductor device. Similarly, for ease of reference, the leakage current in a TFT will be referred to herein as a non-limiting example of the enhanced generation-recombination rate due to trap-to-band tunnelling in a semiconductor device.

Figure 1 hereof is a graph showing voltage current characteristics of a polysilicon TFT. As seen in Fig. 1 when V_{DS} is high (5.1V), the leakage current (I_{DS}) increases with decreasing V_{GS} (below 0V). The magnitude of this leakage current poses as a significant problem, for example, when the TFT is employed as a switching pixel transistor in active matrix LCDs. Several field-assisted generation mechanisms have been proposed to explain this 'off' current.

A quantitative analysis of the leakage current in polysilicon TFTs based on the combination of current-voltage measurements as a function of temperature and 2-D simulations was carried out as long ago as 1995. This analysis shows that the dominant generation mechanism is pure trap-to-band tunnelling below 240K and phonon-assisted trap-to-band tunnelling at higher temperatures. The need to include Poole-Frenkel (PF) barrier lowering in trap-to-band phonon-assisted tunnelling was demonstrated for polysilicon pn junctions as long ago as 1982. Apart from further enhancing the emission rate for trap-to-band phonon-assisted tunnelling, the PF effect also plays a significant role in enhancing pure thermal emissions at low fields.

The PF effect consists of the lowering of a coulombic potential barrier due to the electric field applied to a semiconductor. For a trap to experience the effect, it must be neutral when filled (charged when empty). Such a trap potential is long ranged and is often referred to as a coulombic well. A trap that is neutral when empty will not experience the effect because of the absence of the coulomb potential. Such a trap potential is short ranged and is known as a Dirac well. Without the PF effect, the calculated emission rate is at least one order of magnitude lower than what is needed to fit the experimental data in polysilicon

TFTs. By using a 2-D simulator, based on the known trap-to-band phonon-assisted tunnelling model (Hurkx *et al*) available since 1992, the inventors hereof were unable to simulate the leakage currents in polysilicon TFTs accurately. This is because the conventional model takes only into account Dirac wells and deliberately neglects the PF effect. Moreover, the many attempts at modelling of trap-to-band phonon-assisted tunnelling inclusive of the PF effect, which have been made since development of the original theory by Vincent *et al* in 1979, do not address a key problem: the implementation in a device simulator. The work by Vincent *et al* in 1979 gives evidence both theoretically and experimentally that the electric field in a junction has a large influence on the thermal emission rate of deep levels (mid-gap states). This influence can be quantitatively explained in a model of phonon-assisted tunnelling emission. Tunnelling is very sensitive to the barrier height and is therefore expected to be considerably affected by the PF barrier lowering.

As noted above, in 1996 the present inventors presented a new quantum mechanical tunnelling generation-recombination (G-R) model, conveniently referred to as the Dirac Coulombic Tunnelling Integral, which takes into full rigorous account the PF barrier lowering and is suitable for implementation in a device simulator. This G-R model is consistently formulated for the entire range of electric fields and temperatures. At high fields, the dominant mechanism is found to be trap-to-band phonon-assisted tunnelling inclusive of the PF effect; while at low fields, the model will reduce to that of the standard Shockley-Read-Hall (SRH) thermal G-R.

However, a practical implementation of the model into commercial device simulators has not until this invention been presented despite the length of time since presentation of the Dirac Coulombic Tunnelling Integral and despite the high commercial value of such a practical implementation.

According to a first aspect of the present invention there is provided an automated simulation method for determining enhanced generation recombination rate due to trap-to-band tunnelling in a semiconductor device using the Dirac coulombic tunnelling integral, comprising the steps of:

assigning the variable C to the ratio of the Poole-Frenkel barrier lowering energy (ΔE_ϕ) divided by the energy range for which tunnelling can occur (ΔE_o);

assigning the value (C+1)/2 to a variable v and performing a second order Taylor's series expansion of the Dirac coulombic tunnelling integral around v to determine a maximum value (u_{max}) for the variable u of the integral;

determining if the value for u_{max} is less than C, is between C and 1 or is more than 1;

assigning the value of C to the variable v if u_{max} is less than C;

assigning the value of u_{max} to the variable v if u_{max} is between C and 1;

assigning the value of 1 to the variable v if u_{max} is more than 1;

reducing the Taylor's series expansion of the Dirac coulombic tunnelling integral to an error function;

reducing the error function to simple exponential functions by applying rational approximations to the error function; and

calculating the enhanced generation recombination rate due to trap-to-band tunnelling in a semiconductor device using the said simple exponential functions.

According to a second aspect of the present invention there is provided a simulator for determining enhanced generation recombination rate due to trap-to-band tunnelling in a semiconductor device using the Dirac coulombic tunnelling integral, comprising:

means storing a variable C having a value equal to the ratio of the Poole-Frenkel barrier lowering energy (ΔE_{fp}) divided by the energy range for which tunnelling can occur (ΔE_n);

means which assign the value (C+1)/2 to a variable v and perform a second order Taylor's series expansion of the Dirac coulombic tunnelling integral around v to determine a maximum value (u_{max}) for the variable u of the integral;

means which determine if the value for u_{max} is less than C, is between C and 1 or is more than 1;

means which assign the value of C to the variable v if u_{max} is less than C;

means which assign the value of u_{max} to the variable v if u_{max} is between C and 1;

means which assign the value of 1 to the variable v if u_{max} is more than 1;

means storing simple exponential functions derived from applying rational approximations to an error function obtained by reducing the Taylor's series expansion of the Dirac coulombic tunnelling integral; and

means which calculate the enhanced generation recombination rate due to trap-to-band tunnelling in a semiconductor device using the said simple exponential functions.

Although possible in theory, even with the fastest computers available today, using numerical integration methods to solve the Dirac coulombic tunnelling integral for every trap level in every element in a finite element package will take so much computation time that such an approach can not be used for a commercial and practicable implementation. The present invention enables such a commercial and practicable implementation. Moreover, the present invention can provide high levels of accuracy in the automated modelling of the enhanced generation-recombination rate due to trap-to-band tunnelling in a semiconductor device.

Embodiments of the present invention will now be described in more detail by way of example only and with reference to the accompanying drawings, in which:

Figure 1 is a graph illustrating leakage current in a TFT;

Figure 2 shows two graphs illustrating a low field condition;

Figure 3 shows two graphs illustrating a moderate field condition;

Figure 4 shows two graphs illustrating a high field condition;

Figure 5 is a graph illustrating the performance of the present invention;

Figure 6 is a graph illustrating the performance of the present invention;

Figure 7 is a graph illustrating the performance of the present invention;

Figure 8 is a graph illustrating the performance of the present invention; and

Figure 9 lists equations useful in explaining embodiments of the present invention.

Starting from the Dirac coulombic tunnelling integral, given as Eqn.(1) in figure 9, it is possible for the integral to be expressed in the form shown as Eqn.(2). Applying the simplification shown in Eqn.(3) leads to Eqn.(4). Eqn.(4) can be further simplified to give Eqn.(5), where the function $f(u)$ is as defined in Eqn.(6).

Most of the contribution to the expression of Eqn.(5) can be expected to arise from the condition when the function $f(u)$ is largest. This condition should be considered for the three cases which have distinct characteristics namely, Case 1 when the electric field is low; Case 2 when the electric field is moderate and Case 3 when then the electric field is high. These three distinct conditions are illustrated in figures 2, 3 and 4 respectively.

Figure 2 is based on a low field value (F) of $F = 1x10^7 Vm^{-1}$ for ΔE_n = 0.5eV. The maximum of $f(u)$ occurs at C, giving the maximum contribution to *exp[f(u)]* at C as well.

Figure 3 is based on a moderate field value (F) of $F = 7x10^7 Vm^{-1}$ for ΔE_n = 0.5eV. The maximum of $f(u)$ occurs between C and 1, giving the maximum contribution to *exp[f(u)]* between C and 1 as well.

Figure 4 is based on a high field value (F) of $F = 1x10^8 Vm^{-1}$ for ΔE_n = 0.5eV. The maximum of $f(u)$ occurs at 1, giving the maximum contribution to *exp[f(u)]* at 1 as well.

In a practical implementation it is convenient to consider Case 2 first. That is to determine the u_{max} for maximum $f(u)$ between C and 1. If u_{max} is less than C, then the condition of Case 1 is met. If u_{max} is more than 1 then the condition of Case 3 is met. Using a Taylor's series expansion, $f(u)$ can be approximated by a second-order series expansion around v, where $v = (C+1)/2$ as a reasonable estimate of where u_{max} is likely to occur. Thus is derived Eqn.(7), assuming $f(v)$ is as set out in Eqn.(8) and $f'(v)$ and $f''(v)$ are as set out in Eqn.(9) and Eqn.(10) respectively. Further, this enables $f(u)$ to be rewritten as in Eqn.(11).

From Eqn.(11), $f(u)$ can be differentiated once and the expression equated to zero, to obtain a stationary point, thus following the Eqn.s(12) to obtain a value for u_{max}. If this value of u_{max} is less than C then Case 1 exists. Then it is permissible to set $v = C$ since that is where the maximum $f(u)$ occurs. Then a second order Taylor's series expansion is performed about $v = C$. All of the necessary equations have been established, so it is only necessary to set $v = C$ in the simulator when u_{max} is less than C, so as to obtain an approximate second order expansion of $f(u)$ about C.

If u_{max} is between C and 1, Case 2 exists. In this condition, it is only necessary to set $v = u_{max}$ in the simulator, so as to obtain an approximate second order expansion of $f(u)$ about u_{max}. Here, of course, $v = u_{max}$ is no longer assumed to be equal to (C+1)/2.

If u_{max} is more than 1, Case 3 exists. In this condition, it is only necessary to set $v = 1$ in the simulator, so as to obtain an approximate second order expansion of $f(u)$ about 1.

With the appropriate value of v determined, Eqn.(11) is simplified to lead to Eqn.(13), where *AI*, *AII* and *AIII* are as set out in Eqn.(14), Eqn.(15) and Eqn.(16) respectively.

Completing the square on Eqn.(13) leads to Eqn.(17) and substituting Eqn.(17) into Eqn.(5) gives Eqn.(18). Next a value for t is assigned according to Eqn.(19) and for t_l and t_u when $u = C$ and $u = 1$ according to Eqn.(20) and Eqn.(21) respectively. The value of *du* is as shown by Eqn.(22).

Substitution of Eqn.s(19-22) in to Eqn.(18) leads to Eqn.(23). However, Eqn.(24) is known and a rational approximation thereof gives the function *erf*(x) as set out in Eqn.(25) with the values of t, a_1, a_2, a_3, a_4, a_5 and p as shown.

From Eqn.(24) is finally derived the approximated tunnelling integral according to the method of this embodiment of the present invention and as shown in Eqn.(26), with the values for *AI*, *AII*, *AIII*, t_l, t_u, $f(v)$, $f'(v)$, $f''(v)$, A, B, C, and D as shown. The values of v noted above for Case1, 2 and 3 are also listed for Eqn.(26) as is u_{max} for $v = (C+1)/2$. Of course, u_{max} is solved first in order to determine which of Cases 1, 2 and 3 apply.

An additional term should be respectively added or subtracted in Eqn.(26), as shown in Eqn.(27), if ($t_u > 0$ & $t_l < 0$) or ($t_u < 0$ & $t_l > 0$).

The present invention enables a commercial and practicable implementation of an automated simulation method for determining enhanced generation recombination rate due to trap-to-band tunnelling in a semiconductor device using the Dirac coulombic tunnelling integral. Moreover, the present invention can provide high levels of accuracy in the automated modelling of the enhanced generation-recombination rate due to trap-to-band tunnelling in a semiconductor

device. The method can be implemented in a two-dimensional finite element package.

The present invention uses the characteristics of low, moderate and high field regions with a Taylor's series expansion and a reduction to one or more error functions. Rational approximations are applied to the error functions so as to provide reduction to simple exponential functions. The metod enables cancelling of higher order terms in the exponential functions which otherwise cause premature overflow errors. This enables a much wider range to be calculated, as shown in figure 5.

The method of the invention enables the easy application of proper integration limits so as to ensure a smoth transition between low, moderate and high fields. The effect of removing discontinuities between the low, moderate and high field regions by avoiding conventional simplifications of the integration limits is illustrated in figure 6.

Figure 7 illustrates actual results of an implemention of the present invention for an n-channel polysilicon TFT as compared with the standard SRH model (no field enhancement) and the 1992 model by Hurkx *et al*. It is also to be noted that the implementation of the present invention more accurately simultes the leakage current at low field values (see figure 8 at $V_{DS} = 0.1V$).

Claims

1. An automated simulation method for determining enhanced generation recombination rate due to trap-to-band tunnelling in a semiconductor device using the Dirac coulombic tunnelling integral, comprising the steps of:

assigning the variable C to the ratio of the Poole-Frenkel barrier lowering energy (ΔE_{fp}) divided by the energy range for which tunnelling can occur (ΔE_n);

assigning the value (C+1)/2 to a variable v and performing a second order Taylor's series expansion of the Dirac coulombic tunnelling integral around v to determine a maximum value (u_{max}) for the variable u of the integral;

determining if the value for u_{max} is less than C, is between C and 1 or is more than 1;

assigning the value of C to the variable v if u_{max} is less than C;

assigning the value of u_{max} to the variable v if u_{max} is between C and 1;

assigning the value of 1 to the variable v if u_{max} is more than 1;

reducing the Taylor's series expansion of the Dirac coulombic tunnelling integral to an error function;

reducing the error function to simple exponential functions by applying rational approximations to the error function; and

calculating the enhanced generation recombination rate due to trap-to-band tunnelling in a semiconductor device using the said simple exponential functions.

2. An automated simulation method which determines enhanced generation recombination rate due to trap-to-band tunnelling in a semiconductor device using the approximated tunnelling equation set out as equation 26 herein.

3. An automated simulation method which determines enhanced generation recombination rate due to trap-to-band tunnelling in a semiconductor device using the approximated tunnelling equation set out as equation 27 herein.

4. A simulator as claimed in any one of claims 1 to 3 which determines the leakage current in a polysilicon Thin Film Transistor.

5. A simulator for determining enhanced generation recombination rate due to trap-to-band tunnelling in a semiconductor device using the Dirac coulombic tunnelling integral, comprising:

means storing a variable C having a value equal to the ratio of the Poole-Frenkel barrier lowering energy (ΔE_{tp}) divided by the energy range for which tunnelling can occur (ΔE_t);

means which assign the value (C+1)/2 to a variable v and perform a second order Taylor's series expansion of the Dirac coulombic tunnelling integral around v to determine a maximum value (u_{max}) for the variable u of the integral;

means which determine if the value for u_{max} is less than C, is between C and 1 or is more than 1;

means which assign the value of C to the variable v if u_{max} is less than C;

means which assign the value of u_{max} to the variable v if u_{max} is between C and 1;

means which assign the value of 1 to the variable v if u_{max} is more than 1;

means storing simple exponential functions derived from applying rational approximations to an error function obtained by reducing the Taylor's series expansion of the Dirac coulombic tunnelling integral; and

means which calculate the enhanced generation recombination rate due to trap-to-band tunnelling in a semiconductor device using the said simple exponential functions.

6. A simulator which determines enhanced generation recombination rate due to trap-to-band tunnelling in a semiconductor device comprising means which calculate the approximated tunnelling equation set out as equation 26 herein.

7. A simulator which determines enhanced generation recombination rate due to trap-to-band tunnelling in a semiconductor device comprising means which calculate the approximated tunnelling equation set out as equation 27 herein.

8. A simulator as claimed in any one of claims 5 to 7 which determines the leakage current in a polysilicon Thin Film Transistor.

Abstract

An automated simulation method for determining the enhanced generation-recombination rate due to trap-to-band tunnelling in a semiconductor device using the Dirac coulombic tunnelling integral and to a simulator for carrying out the method are disclosed. The method and simulator are, for example, particularly useful in the modelling of characteristics such as leakage current in polysilicon TFTs, which leakage current can, for example, seriously degrade pixel voltage in active matrix display devices. The simulator embodies the method, which method comprises the steps of: assigning the variable C to the ratio of the Poole-Frenkel barrier lowering energy (ΔE_{tp}) divided by the energy range for which tunnelling can occur (ΔE_n); assigning the value (C+1)/2 to a variable v and performing a second order Taylor's series expansion of the Dirac coulombic tunnelling integral around v to determine a maximum value (u_{max}) for the variable u of the integral; determining if the value for u_{max} is less than C, is between C and 1 or is more than 1; assigning the value of C to the variable v if u_{max} is less than C; assigning the value of u_{max} to the variable v if u_{max} is between C and 1; assigning the value of 1 to the variable v if u_{max} is more than 1; reducing the Taylor's series expansion of the Dirac coulombic tunnelling integral to an error function; reducing the error function to simple exponential functions by applying rational approximations to the error function; and calculating the enhanced generation recombination rate due to trap-to-band tunnelling in a semiconductor device using the said simple exponential functions.

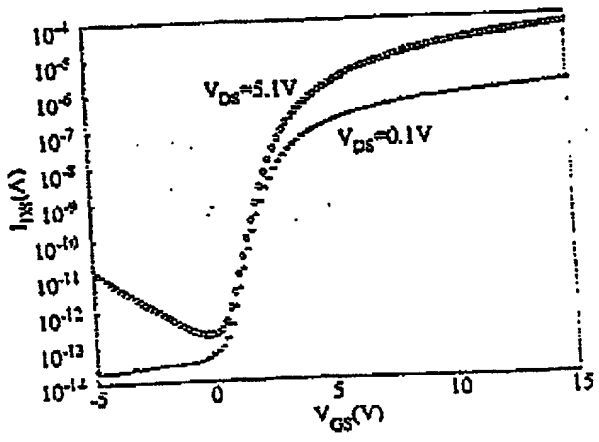
V_{DS}=5.1V
V_{DS}=0.1V
I_{DS}(A)
V_{GS}(V)

Fig. 1

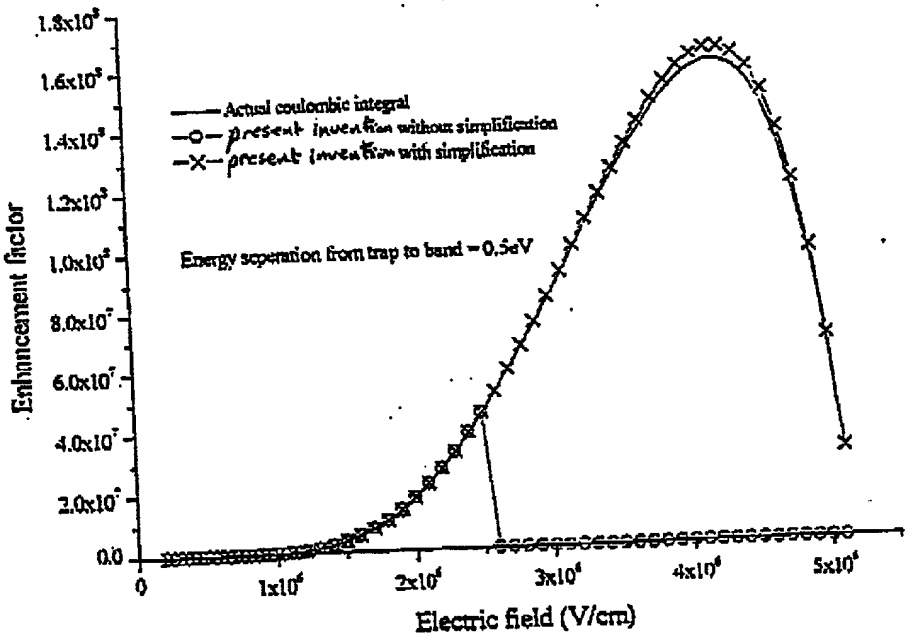
Actual coulombic integral
present invention without simplification
present invention with simplification
Energy seperation from trap to band = 0.5eV
Enhancement factor
Electric field (V/cm)

Fig. 5

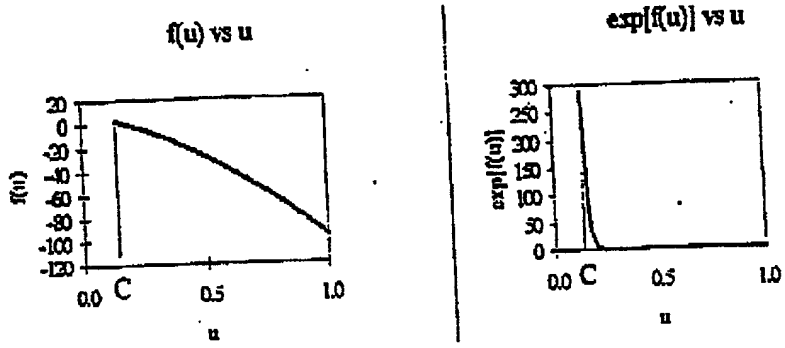

Fig. 2

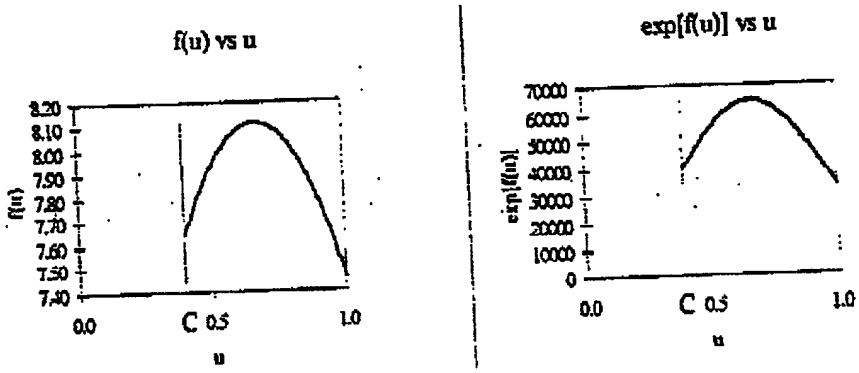

Fig. 3

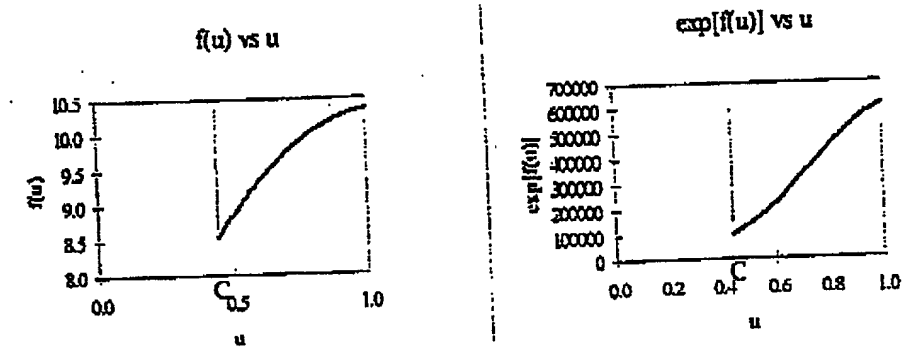

Fig. 4

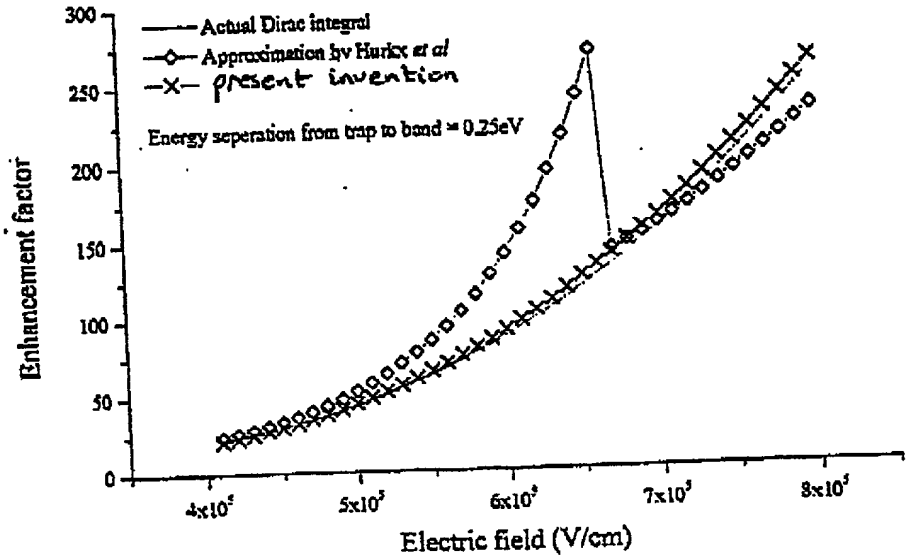
Actual Dirac integral
Approximation by Hurkx et al
present invention
Energy seperation from trap to band = 0.25eV
Enhancement factor
Electric field (V/cm)
300
250
200
150
100
50
0
4x10^5
5x10^5
6x10^5
7x10^5
8x10^5

Fig. 6

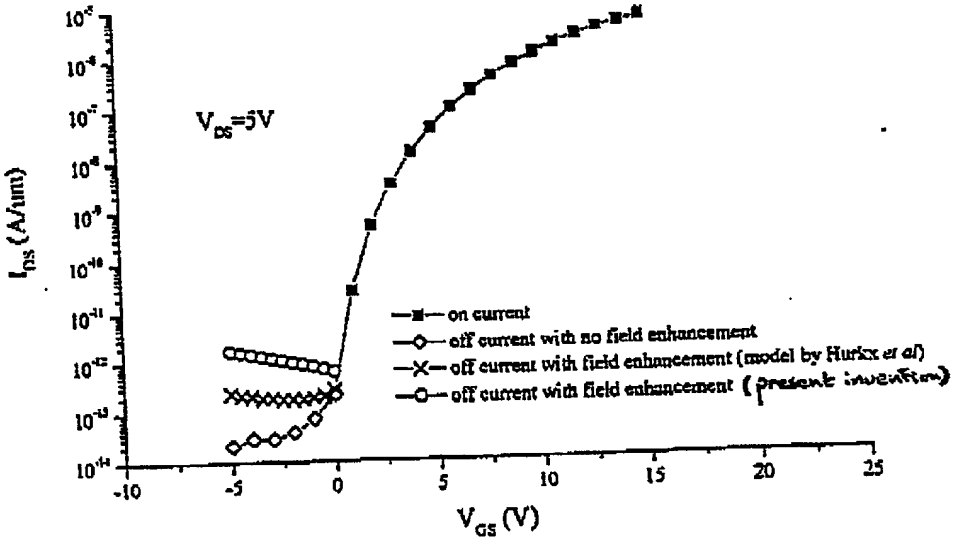
V_DS=5V
I_DS (A/um)
V_GS (V)
on current
off current with no field enhancement
off current with field enhancement (model by Hurkx et al)
off current with field enhancement (present invention)
-10
-5
0
5
10
15
20
25

Fig. 7

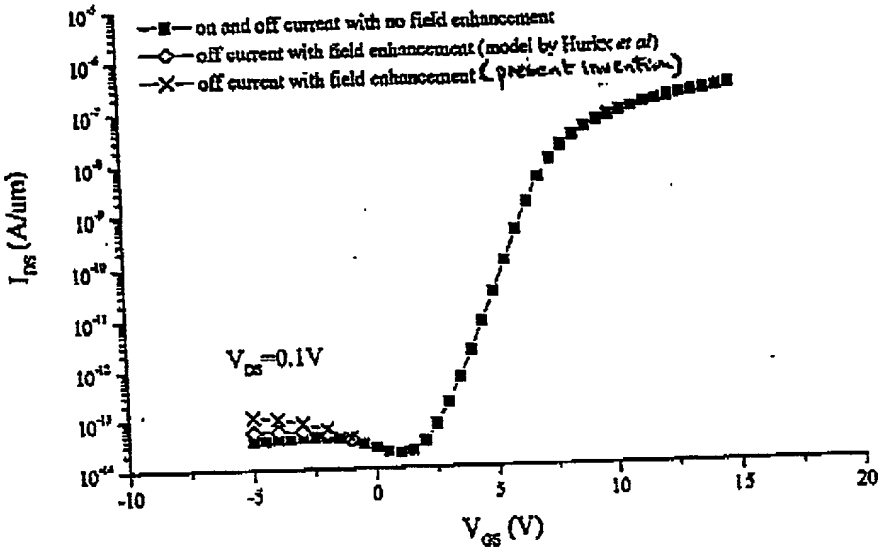
on and off current with no field enhancement
off current with field enhancement (model by Hurkx et al)
off current with field enhancement (present invention)
I_{DS} (A/um)
V_{DS}=0.1V
V_{GS} (V)
-10
-5
0
5
10
15
20

Fig. 8

$$\Gamma_n^{Coul} = \frac{\Delta E_n}{kT} \int_{\frac{\Delta E_{fp}}{\Delta E_n}}^{1} \exp\left\{ \frac{\Delta E_n}{kT} u - K_n u^{\frac{3}{2}} \left[1 - \left(\frac{\Delta E_{fp}}{u \Delta E_n} \right)^{\frac{5}{3}} \right] \right\} du \tag{1}$$

$$\Gamma_n^{Coul} = \frac{\Delta E_n}{kT} \int_{\frac{\Delta E_{fp}}{\Delta E_n}}^{1} \exp\left\{ \frac{\Delta E_n}{kT} u - K_n u^{\frac{3}{2}} + K_n \left(\frac{\Delta E_{fp}}{\Delta E_n} \right)^{\frac{5}{3}} u^{\frac{1}{6}} \right\} du . \tag{2}$$

$$A = \frac{\Delta E_n}{kT}, B = K_n, C = \frac{\Delta E_{fp}}{\Delta E_n}, D = BC^{\frac{5}{3}} . \tag{3}$$

$$\Gamma_n^{Coul} = A \int_C^1 \exp\left\{ Au - Bu^{\frac{3}{2}} + Du^{\frac{1}{6}} \right\} du . \tag{4}$$

$$\Gamma_n^{Coul} = A \int_C^1 \exp[f(u)] du \tag{5}$$

$$f(u) = Au - Bu^{\frac{3}{2}} + Du^{\frac{1}{6}} . \tag{6}$$

$$f(u) \approx f(v) + f'(v)(u - v) + \frac{f''(v)}{2}(u - v)^2 , \tag{7}$$

$$f(v) = Av - Bv^{\frac{3}{2}} + Dv^{\frac{1}{6}} , \tag{8}$$

$$f'(v) = A - \frac{3}{2} Bv^{\frac{1}{2}} - \frac{1}{6} Dv^{-\frac{7}{6}} \tag{9}$$

$$f''(v) = -\frac{3}{4} Bv^{-\frac{1}{2}} + \frac{7}{36} Dv^{-\frac{13}{6}} . \tag{10}$$

$$f(u) \approx \frac{f''(v)}{2} u^2 + [f'(v) - vf''(v)] u + \left[v^2 \frac{f''(v)}{2} - vf'(v) + f(v) \right] . \tag{11}$$

$$f'(u) \approx f''(v)u + [f'(v) - vf''(v)] = 0\,,$$ (11) cont.

$$u_{max} = \frac{f'(v) - vf''(v)}{f''(v)}\,.$$ (12)

$$f(u) \approx -(AIu^2 + AIIu + AIII)$$ (13)

$$AI = -\frac{f''(v)}{2}\,,$$ (14)

$$AII = -[f'(v) - vf''(v)]$$ (15)

$$AIII = -\left[v^2\frac{f''(v)}{2} - vf'(v) + f(v)\right].$$ (16)

$$f(u) \approx -AI\left[\left(u + \frac{AII}{2AI}\right)^2 + \left(\frac{AIII}{AI} - \left(\frac{AII}{2AI}\right)^2\right)\right].$$ (17)

$$\Gamma_n^{Coul} = A\int_C^1 \exp[f(u)]du$$

$$\Gamma_n^{Coul} = A\exp - \left[AI\left(\frac{AIII}{AI} - \left(\frac{AII}{2AI}\right)^2\right)\right]\int_C^1 \exp - \left[\sqrt{AI}\left(u + \frac{AII}{2AI}\right)\right]^2 du\,.$$ (18)

$$t = \sqrt{AI}\left(u + \frac{AII}{2AI}\right),$$ (19)

$$u = C,\ t_l = \sqrt{AI}\left(C + \frac{AII}{2AI}\right),$$ (20)

$$u = 1,\ t_u = \sqrt{AI}\left(1 + \frac{AII}{2AI}\right),$$ (21)

$$du = \frac{1}{\sqrt{AI}}dt\,.$$ (22)

$$\Gamma_n^{Coul} = \frac{A}{\sqrt{AI}}\exp - \left[AI\left(\frac{AIII}{AI} - \left(\frac{AII}{2AI}\right)^2\right)\right]\int_{t_l}^{t_u} e^{-t^2}dt\,.$$ (23)

$$\int_{t_1}^{t_u} e^{-x^2}\,dt = \frac{\sqrt{\pi}}{2}\left[erf(t_u) - erf(t_1)\right]. \tag{24}$$

$$erf(x) = 1 - \left(a_1 t + a_2 t^2 + a_3 t^3 + a_4 t^4 + a_5 t^5\right) e^{-x^2},$$

$$t = \frac{1}{1 + px},$$

a_1=0.254829592;
a_2=-0.284496736;
a_3=1.421413741;
a_4=-1.453152027;
a_5=1.061405429;
p=0.3275911; (25)

$$\Gamma_n^{Coul} = \frac{A}{2}\sqrt{\frac{\pi}{AI}}\left(\frac{a_1}{(1+pt_1)} + \frac{a_2}{(1+pt_1)^2} + \frac{a_3}{(1+pt_1)^3} + \frac{a_4}{(1+pt_1)^4} + \frac{a_5}{(1+pt_1)^5}\right)\exp\left(-C^2 AI - CAII - AIII\right)$$
$$-\frac{A}{2}\sqrt{\frac{\pi}{AI}}\left(\frac{a_1}{(1+pt_u)} + \frac{a_2}{(1+pt_u)^2} + \frac{a_3}{(1+pt_u)^3} + \frac{a_4}{(1+pt_u)^4} + \frac{a_5}{(1+pt_u)^5}\right)\exp\left(-AI - AII - AIII\right) \tag{26}$$

$$AI = -\frac{f''(v)}{2},\quad AII = -\left[f'(v) - vf''(v)\right],\quad AIII = -\left[v^2\frac{f''(v)}{2} - vf'(v) + f(v)\right],$$

$$t_1 = \sqrt{AI}\left(C + \frac{AII}{2AI}\right),\quad t_u = \sqrt{AI}\left(1 + \frac{AII}{2AI}\right).$$

$$f(v) = Av - Bv^{\frac{3}{2}} + Dv^{-\frac{1}{4}},$$

$$f'(v) = A - \frac{3}{2}Bv^{\frac{1}{2}} - \frac{1}{6}Dv^{-\frac{7}{6}},$$

$$f''(v) = -\frac{3}{4}Bv^{-\frac{1}{2}} + \frac{7}{36}Dv^{-\frac{13}{6}},$$

$$A=\frac{\Delta E_n}{kT}, B=K_n, C=\frac{\Delta E_{fb}}{\Delta E_n}, D=BC^{\frac{5}{3}},$$

$v = C$ (for $u_{max} < C$, case 1),

$v = u_{max}$ (for $C < u_{max} < 1$, case 2),

$v = 1$ (for $u_{max} \geq 1$, case 3),

$$u_{max}=\frac{f'(v)-vf''(v)}{f''(v)} \text{ for } v=\frac{C+1}{2}.$$

$$\Gamma_n^{Coul}=\frac{A}{2}\sqrt{\frac{\pi}{AI}}\left(\frac{a_1}{(1+pt_l)}+\frac{a_2}{(1+pt_l)^2}+\frac{a_3}{(1+pt_l)^3}+\frac{a_4}{(1+pt_l)^4}+\frac{a_5}{(1+pt_l)^5}\right)\exp\left(-C^2AI-CAII-AIII\right)$$
$$-\frac{A}{2}\sqrt{\frac{\pi}{AI}}\left(\frac{a_1}{(1+pt_u)}+\frac{a_2}{(1+pt_u)^2}+\frac{a_3}{(1+pt_u)^3}+\frac{a_4}{(1+pt_u)^4}+\frac{a_5}{(1+pt_u)^5}\right)\exp\left(-AI-AII-AIII\right)$$
$$\pm A\sqrt{\frac{\pi}{AI}}\exp\left(-AIII+\frac{AII^2}{4AI}\right)$$

(27)

DECLARATION AND POWER OF ATTORNEY
UNDER 35 USC §371(c)(4) FOR
PCT APPLICATION FOR UNITED STATES PATENT

As a below named inventor, I hereby declare that:
my residence, post office address and citizenship are as stated below under my name;

I verily believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought, namely the invention entitled: Semiconductor Device Simulation Method and Simulator

described and claimed in international application number _____ filed _____.

I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

Under Title 35, U.S. Code §119, the priority benefits of the following foreign application(s) filed by me or my legal representatives or assigns within one year prior to my international application are hereby claimed:

The following application(s) for patent or inventor's certificate on this invention were filed in countries foreign to the United States of America either (a) more than one year prior to my international application, or (b) before the filing date of the above-named foreign priority application(s):

I hereby appoint the following as my attorneys of record with full power of substitution and revocation to prosecute this application and to transact all business in the Patent Office:

James A. Oliff, Reg. No. 27,075; William P. Berridge, Reg. No. 30,024;
Kirk M. Hudson, Reg. No. 27,562; Thomas J. Pardini, Reg. No. 30,411;
Edward P. Walker, Reg. No. 31,450; Robert A. Miller, Reg. No. 32,771;
Mario A. Costantino, Reg. No. 33,565; Stephen J. Roe, Reg. No. 34,463;
Joel S. Armstrong, Reg. No. 36,430; Christopher W. Brown, Reg. No. 38,025; and
Richard E. Rice, Reg. No. 31,560.

ALL CORRESPONDENCE IN CONNECTION WITH THIS APPLICATION SHOULD BE SENT TO OLIFF & BERRIDGE, PLC, P.O. BOX 19928, ALEXANDRIA, VIRGINIA 22320, TELEPHONE (703) 836-6400.

I hereby declare that I have reviewed and understand the contents of this Declaration, and that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

1	*Typewritten Full Name of Sole or First Inventor*	Basil		Lui
		Given Name	Middle Initial	Family Name
2	Inventor's Signature	X Basil		
3	Date of Signature	X March 15 2001		
		Month	Day	Year
	Residence:	Cambridge, Great Britain GBN		
		City	State or Province	Country
	Citizenship:	British		
	Post Office Address: (Insert complete mailing address, including country)	8c Kings Parade Cambridge, Great Britain		

Note to Inventor: Please sign name on line 2 exactly as it appears in line 1 and insert the actual date of signing on line 3.

TOTAL P.02